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<b>TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT</b> (Under 37 CFR 1.97(b) or 1.97(c))		Docket No. <b>BUR920040075US1</b>	
In Re Application Of: <b>EEC E. Foreman et al.</b>			
Serial No. <b>10/709,361</b>	Filing Date <b>04/29/2004</b>	Examiner <b>Unassigned</b>	Group Art Unit <b>Unassigned</b>
Title: <b>METHOD AND SYSTEM FOR EVALUATING TIMING IN AN INTEGRATED CIRCUIT</b>			
<p>Address to:</p> <p><b>Commissioner for Patents</b> <b>P.O. Box 1450</b> <b>Alexandria, VA 22313-1450</b></p> <p><b>37 CFR 1.97(b)</b></p> <p>1. <input checked="" type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.</p> <p style="text-align: center;"><b>37 CFR 1.97(c)</b></p> <p>2. <input type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:</p> <p style="margin-left: 40px;"><input type="checkbox"/> the statement specified in 37 CFR 1.97(e);</p> <p style="text-align: center; margin: 10px 0;"><b>OR</b></p> <p style="margin-left: 40px;"><input type="checkbox"/> the fee set forth in 37 CFR 1.17(p).</p>			

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.  
**BUR920040075US1**

In Re Application: **Eric E. Foreman et al.**

Serial No.

10/709,361

Filing Date

04/29/2004

Examiner

Unassigned

Group Art Unit

Unassigned

**METHOD AND SYSTEM FOR EVALUATING TIMING IN AN INTEGRATED CIRCUIT**

**Payment of Fee**

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.
- ☐ Charge the amount of \_\_\_\_\_
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.

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I certify that this document and authorization to charge deposit account is being facsimile transmitted to the United States Patent and Trademark Office (F:

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**Certificate of Mailing by First Class Mail**

I certify that this document and fee is being deposited on **05/12/04** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

\_\_\_\_\_  
Signature of Person Mailing Correspondence

C. Mueller

\_\_\_\_\_  
Typed or Printed Name of Person Mailing Certificate

**\*This certificate may only be used if paying by deposit account.**

\_\_\_\_\_  
Signature

**Richard M. Kotulak, Reg. #27712**  
**IP Law Department, 972E**  
**IBM Corporation**  
**1000 River Street**  
**Essex Junction, VT 05452**  
**Telephone: 802-769-4457**

Dated: **5/10/04**

CC:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Eric A. Foreman, et al.

Group Art Unit: Unknown

Serial No.: ~~Not assigned yet~~ 10/709,361

Examiner: Unknown

Filed: ~~Concurrently herewith~~ 04/29/2004

For: **METHOD AND SYSTEM FOR EVALUATING TIMING IN AN INTEGRATED CIRCUIT**

MAIL STOP PATENT APPLICATION

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. 1.56**

Sir:

Under the provisions of 37 C.F.R. §§ 1.97 and 1.98, and pursuant to Applicants' duty of disclosure under 37 C.F.R. § 1.56, Applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the cited references is enclosed for the Examiner's convenience.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. The references are merely cited as constituting related art of which the Applicants are aware.

It is respectfully requested that these documents be considered by the Examiner and formally made of record in this application. Applicants also respectfully request that an initialed copy of the Form PTO-1449 be returned along with the next Office Action to confirm that the cited references have been considered.

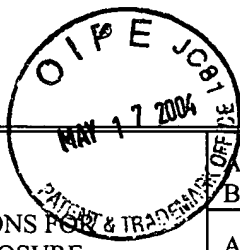
Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Andrew M. Calderon', with a stylized, cursive script.

Andrew M. Calderon  
Reg. No. 38,093

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FORM PTO-1449 (Modified)	ATTY. DOCKET NO. BUR920040075US1	SERIAL NO. Unassigned 10/709,361
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Eric A. Foreman, et al.	
(Use several sheets if necessary)	FILING DATE: 04/29/04 <del>Concurrently Herewith</del>	GROUP: Unassigned

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	Aseem Agarwal, et al., "Statistical Timing Analysis for Intra-Die Process Variations with Spatial Correlations," ICCAD '03, November 11-13, 2003, pages 621-625.
	Hongliang Chang, et al., "Statistical Timing Analysis Considering Spatial Correlations Using a Single Pert-Like Traversal," ICCAD '03, November 11-13, 2003, pages 900-907.
	Michael Orshansky, et al., "Impact of Spatial Intrachip Gate Length Variability on the Performance of High-Speed Digital Circuits," IBEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 5, May 2002, pages 544-553.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.